1.2 W audio power amplifier with active-low standby mode

Features

- Operating range from V_{CC} = 2.2 V to 5.5 V
- 1.2 W output power at V_{CC} = 5 V, THD = 1%, F = 1 kHz, with 8 Ω load
- Ultra-low consumption in standby mode (10 nA)
- 62 dB PSRR at 217 Hz in grounded mode
- Near-zero pop and click
- Ultra-low distortion (0.1%)
- Unity gain stable
- Available in 9-bump flip-chip, miniSO-8 and DFN8 packages

Applications

- Mobile phones (cellular / cordless)
- Laptop / notebook computers
- PDAs
- Portable audio devices

Description

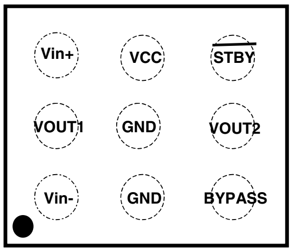
The TS4990 is designed for demanding audio applications such as mobile phones to reduce the number of external components.

This audio power amplifier is capable of delivering 1.2 W of continuous RMS output power into an 8 Ω load at 5 V.

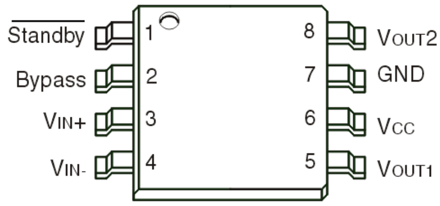
An externally controlled standby mode reduces the supply current to less than 10 nA. It also includes an internal thermal shutdown protection.

The unity-gain stable amplifier can be configured by external gain setting resistors.

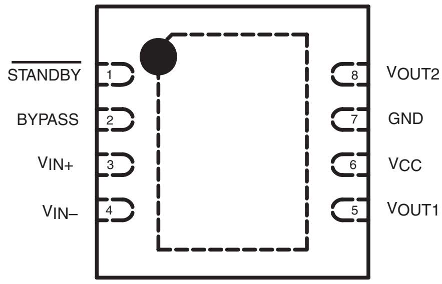
TS4990IJT/TS4990EIJT - Flip-chip 9 bumps



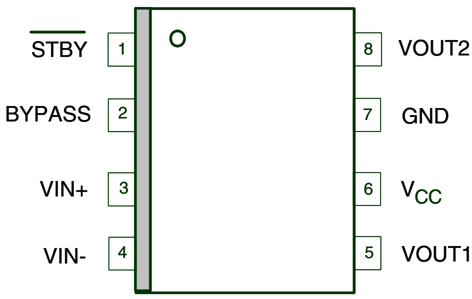
TS4990IST - MiniSO-8



TS4990IQT - DFN8



TS4990ID/TS4990IDT - SO-8



Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
V_{in}	Input voltage [2]	GND to V_{CC}	V
T_{oper}	Operating free-air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient Flip-chip [3] MiniSO-8 DFN8	 250 215 120	°C/W
P_{diss}	Power dissipation	Internally limited	
ESD	HBM: Human body model[4] MM: Machine model[5]	2 200	kV V
	Latch-up immunity	200	mA
	Lead temperature (soldering, 10sec) Lead temperature (soldering, 10sec) for lead-free version	250 260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V.
3. The device is protected in case of over temperature by a thermal shutdown active at 150° C.
4. Human body model: A 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
5. Machine model: A 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.2 to 5.5	V
V_{icm}	Common mode input voltage range	1.2V to V_{CC}	V
V_{STBY}	Standby voltage input: Device ON Device OFF	 $1.35 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
R_L	Load resistor	≥ 4	Ω
T_{SD}	Thermal shutdown temperature	150	°C
R_{thja}	Thermal resistance junction to ambient Flip-chip [1] MiniSO-8 DFN8[2]	 100 190 40	°C/W

1. This thermal resistance is reached with a 100 mm^2 copper heatsink surface.
2. When mounted on a 4-layer PCB.

2 Typical application schematics

Figure 1. Typical application schematics

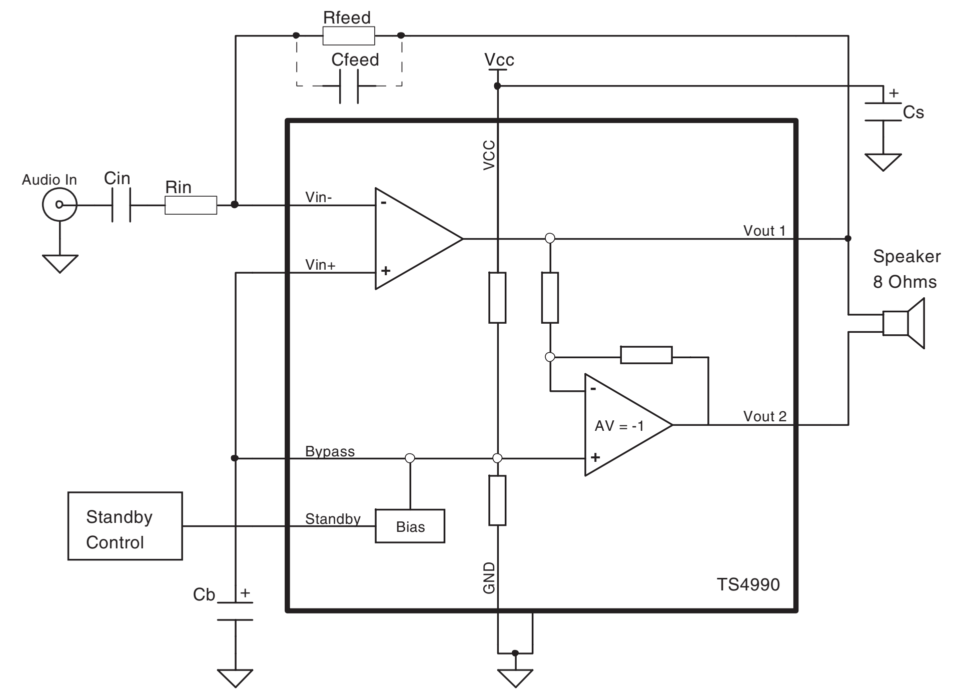


Table 3. Component descriptions

Component	Functional description
R_{in}	Inverting input resistor that sets the closed loop gain in conjunction with R_{feed}. This resistor also forms a high pass filter with C_{in} ($F_c = 1 / (2 \times Pi \times R_{in} \times C_{in})$).
C_{in}	Input coupling capacitor that blocks the DC voltage at the amplifier input terminal.
R_{feed}	Feed back resistor that sets the closed loop gain in conjunction with R_{in}.
C_s	Supply bypass capacitor that provides power supply filtering.
C_b	Bypass pin capacitor that provides half supply filtering.
C_{feed}	Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency 1/ (2 x Pi x R_{feed} x C_{feed})).
A_V	Closed loop gain in BTL configuration = 2 x (R_{feed} / R_{in}).
Exposed pad	DFN8 exposed pad is electrically connected to pin 7. See *DFN8 package information on page 29* for more information.

3 Electrical characteristics

Table 4. Electrical characteristics when V_{CC} = +5 V, GND = 0 V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		3.7	6	mA
I_{STBY}	Standby current (1) No input signal, V_{STBY} = GND, R_L = 8Ω		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		1	10	mV
P_{out}	Output power THD = 1% max, F = 1kHz, R_L = 8 Ω	0.9	1.2		W
THD + N	Total harmonic distortion + noise P_{out} = 1W_{rms}, A_V = 2, 20Hz ≤ F ≤ 20kHz, R_L = 8 Ω		0.2		%
PSRR	Power supply rejection ratio(2) R_L = 8 Ω, A_V = 2, V_{ripple} = 200mV_{pp}, input grounded F = 217Hz F = 1kHz	 55 55	 62 64		dB
t_{WU}	Wake-up time (C_b = 1 µF)		90	130	ms
t_{STBY}	Standby time (C_b = 1 µF)		10		µs
V_{STBYH}	Standby voltage level high			1.3	V
V_{STBYL}	Standby voltage level low			0.4	V
Φ_M	Phase margin at unity gain R_L = 8 Ω, C_L = 500 pF		65		Degrees
GM	Gain margin R_L = 8 Ω, C_L = 500 pF		15		dB
GBP	Gain bandwidth product R_L = 8 Ω		1.5		MHz
$R_{OUT-GND}$	Resistor output to GND ($V_{STBY} \leq V_{STBYL}$) V_{out1} V_{out2}		 3 43		kΩ

1. Standby mode is active when V_{STBY} is tied to GND.
2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon V_{CC}.

Table 5. Electrical characteristics when V_{CC} = +3.3 V, GND = 0 V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		3.3	6	mA
I_{STBY}	Standby current [1] No input signal, V_{STBY} = GND, R_L = 8 Ω		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		1	10	mV
P_{out}	Output power THD = 1% max, F = 1 kHz, R_L = 8 Ω	375	500		mW
THD + N	Total harmonic distortion + noise P_{out} = 400 mW_{rms}, A_V = 2, 20 Hz ≤ F ≤ 20 kHz, R_L = 8 Ω		0.1		%
PSRR	Power supply rejection ratio[2] R_L = 8 Ω, A_V = 2, V_{ripple} = 200mV_{pp}, input grounded F = 217 Hz F = 1 kHz	 55 55	 61 63		dB
t_{WU}	Wake-up time (C_b = 1 µF)		110	140	ms
t_{STBY}	Standby time (C_b = 1 µF)		10		µs
V_{STBYH}	Standby voltage level high			1.2	V
V_{STBYL}	Standby voltage level low			0.4	V
Φ_M	Phase margin at unity gain R_L = 8 Ω, C_L = 500 pF		65		Degrees
GM	Gain margin R_L = 8 Ω, C_L = 500 pF		15		dB
GBP	Gain bandwidth product R_L = 8 Ω		1.5		MHz
$R_{OUT\text{-}GND}$	Resistor output to GND (V_{STBY} ≤ V_{STBYL}) V_{out1} V_{out2}		 4 44		kΩ

1. Standby mode is active when V_{STBY} is tied to GND.
2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon V_{CC}.

Table 6. Electrical characteristics when V_{CC} = 2.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		3.1	6	mA
I_{STBY}	Standby current [(1)] No input signal, V_{STBY} = GND, R_L = 8 Ω		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		1	10	mV
P_{out}	Output power THD = 1% max, F = 1 kHz, R_L = 8 Ω	220	300		mW
THD + N	Total harmonic distortion + noise P_{out} = 200 mW_{rms}, A_V = 2, 20 Hz ≤ F ≤ 20 kHz, R_L = 8 Ω		0.1		%
PSRR	Power supply rejection ratio[(2)] R_L = 8 Ω, A_V = 2, V_{ripple} = 200 mV_{pp}, input grounded F = 217 Hz F = 1 kHz	 55 55	 60 62		dB
t_{WU}	Wake-up time (C_b = 1 µF)		125	150	ms
t_{STBY}	Standby time (C_b = 1 µF)		10		µs
V_{STBYH}	Standby voltage level high			1.2	V
V_{STBYL}	Standby voltage level low			0.4	V
Φ_M	Phase margin at unity gain R_L = 8 Ω, C_L = 500 pF		65		Degrees
GM	Gain margin R_L = 8 Ω, C_L = 500 pF		15		dB
GBP	Gain bandwidth product R_L = 8 Ω		1.5		MHz
$R_{OUT\text{-}GND}$	Resistor output to GND ($V_{STBY} \leq V_{STBYL}$) V_{out1} V_{out2}		 6 46		kΩ

1. Standby mode is active when V_{STBY} is tied to GND.
2. All PSRR data limits are guaranteed by production sampling tests.
Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon V_{CC}.

Figure 2. Open loop frequency response

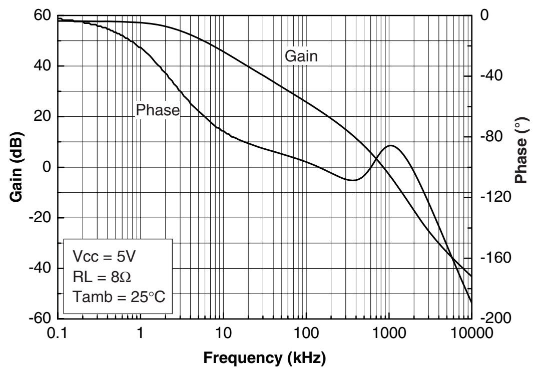


Figure 3. Open loop frequency response

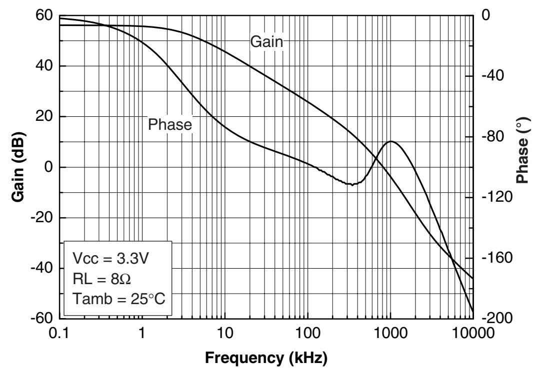


Figure 4. Open loop frequency response

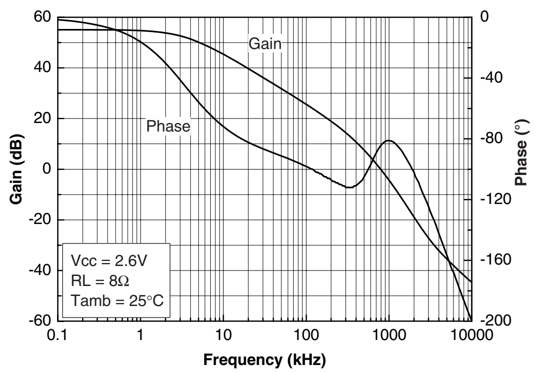


Figure 5. Open loop frequency response

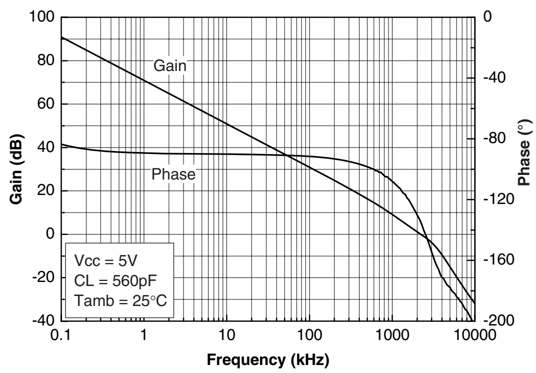


Figure 6. Open loop frequency response

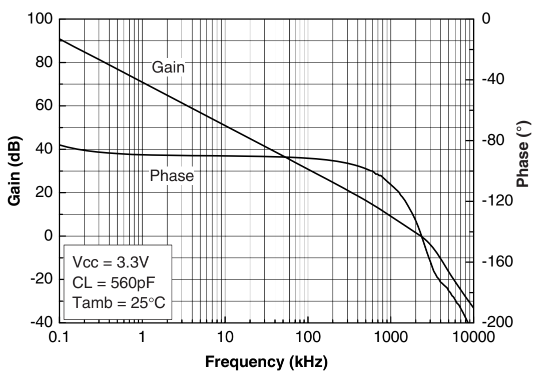


Figure 7. Open loop frequency response

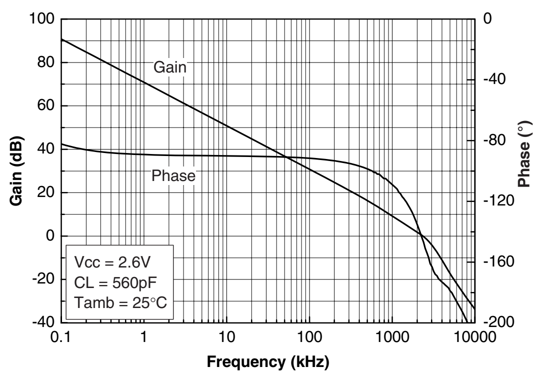


Figure 8. PSRR vs. power supply

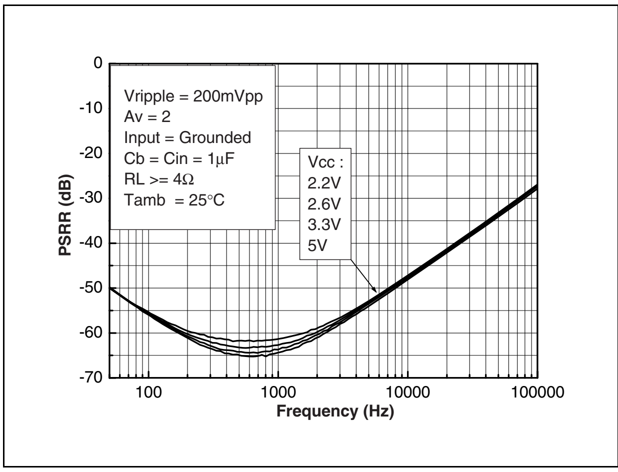


Figure 9. PSRR vs. power supply

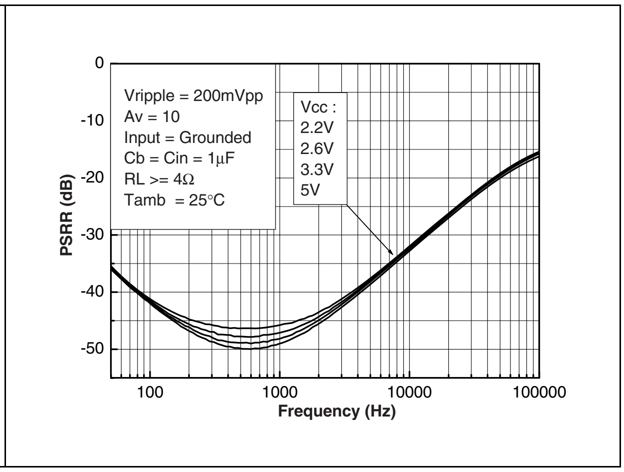


Figure 10. PSRR vs. power supply

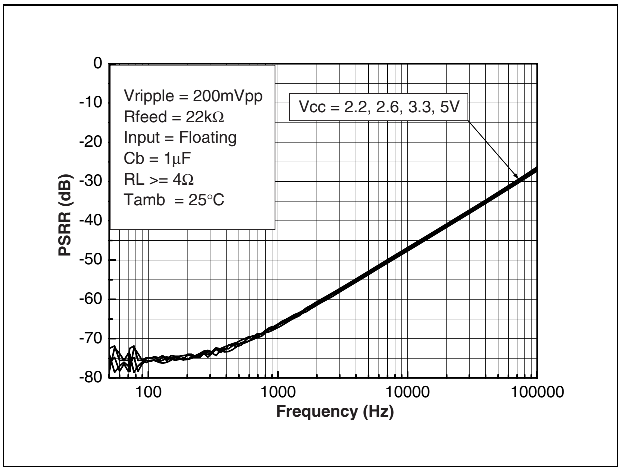


Figure 11. PSRR vs. power supply

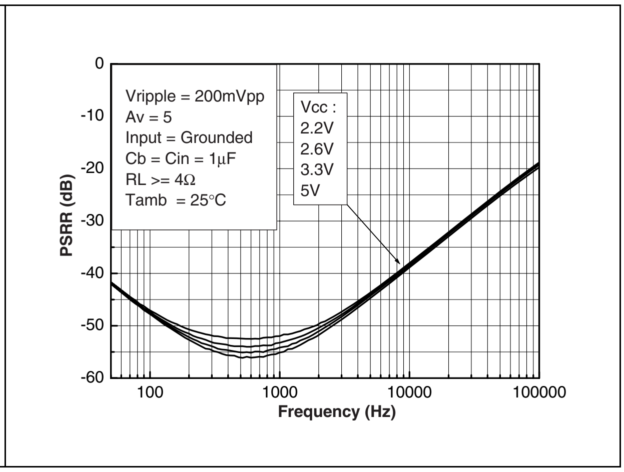


Figure 12. PSRR vs. power supply

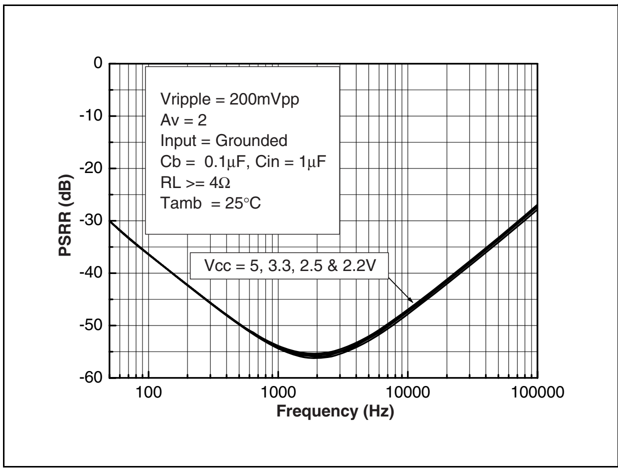


Figure 13. PSRR vs. power supply

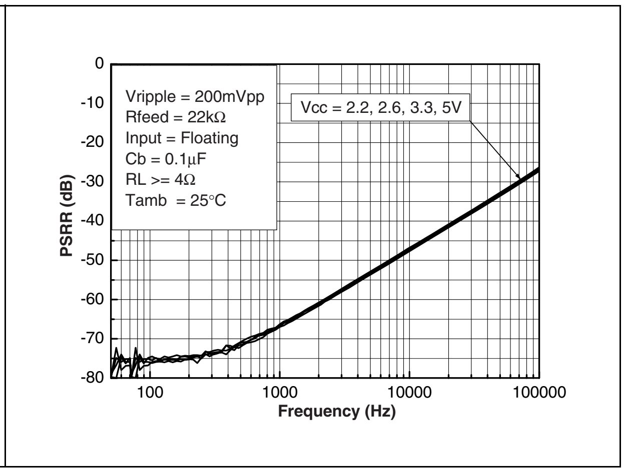


Figure 14. PSRR vs. DC output voltage

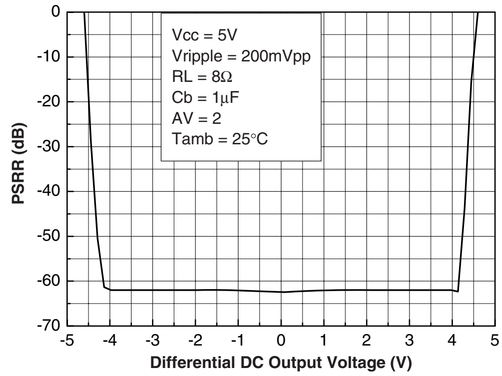


Figure 15. PSRR vs. DC output voltage

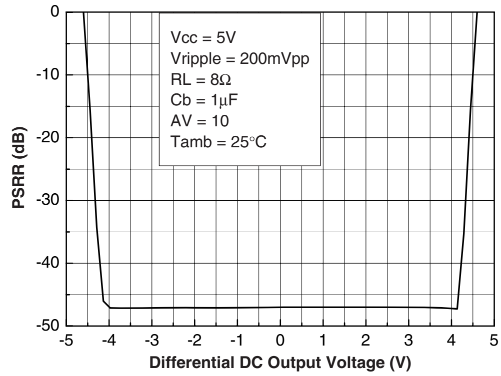


Figure 16. PSRR vs. DC output voltage

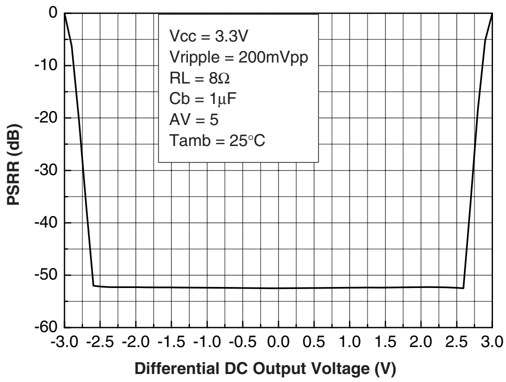


Figure 17. PSRR vs. DC output voltage

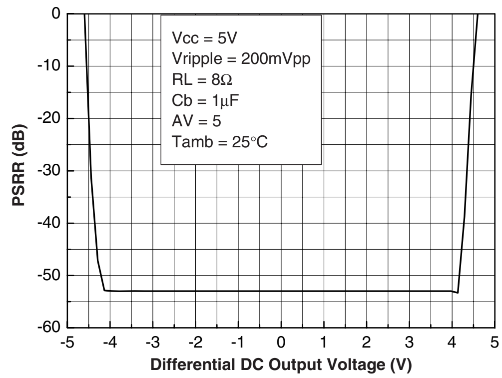


Figure 18. PSRR vs. DC output voltage

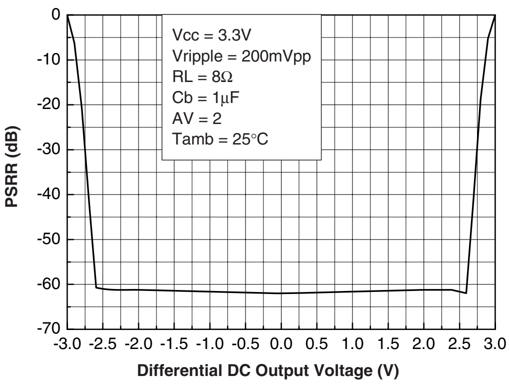


Figure 19. PSRR vs. DC output voltage

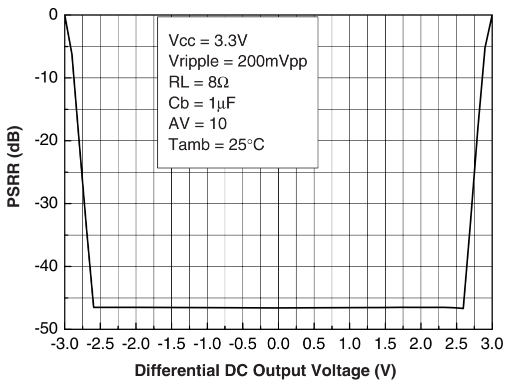


Figure 20. PSRR vs. DC output voltage

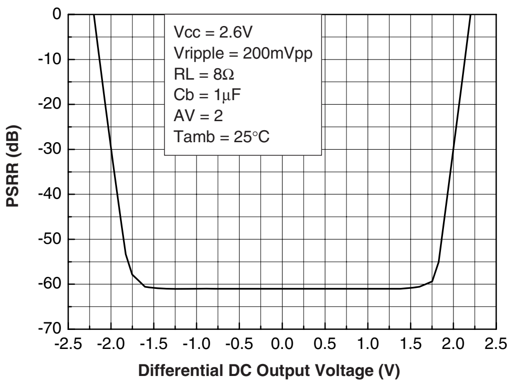


Figure 21. PSRR vs. DC output voltage

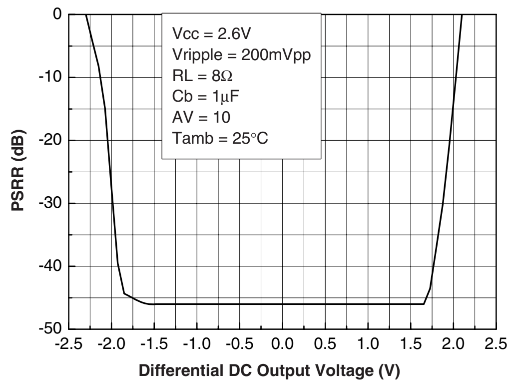


Figure 22. Output power vs. power supply voltage

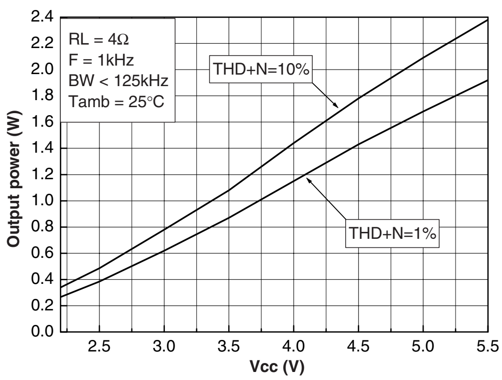


Figure 23. PSRR vs. DC output voltage

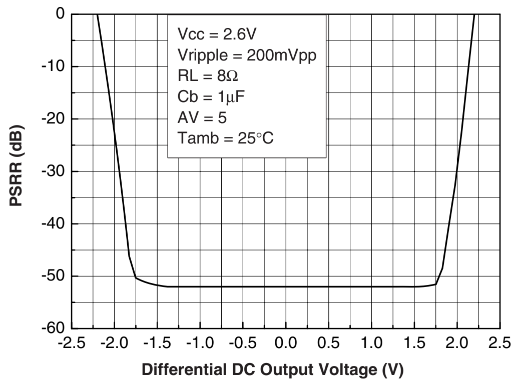


Figure 24. PSRR at F = 217 Hz vs. bypass capacitor

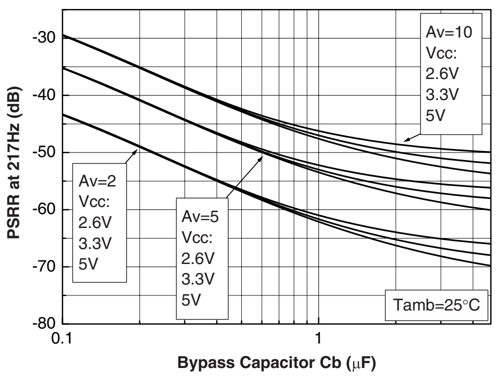


Figure 25. Output power vs. power supply voltage

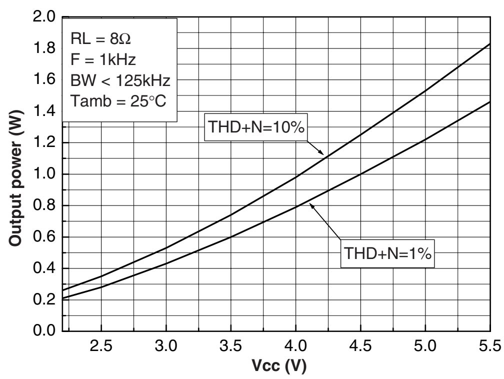


Figure 26. Output power vs. power supply voltage

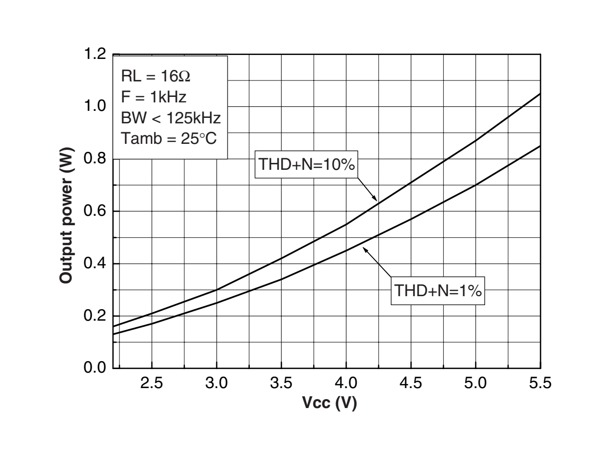


Figure 27. Output power vs. load resistor

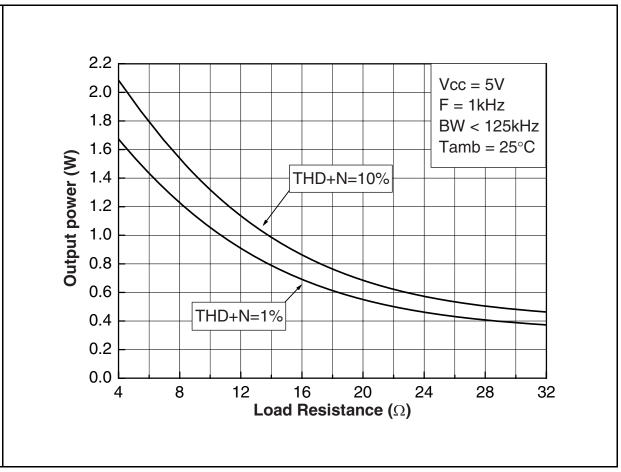


Figure 28. Output power vs. load resistor

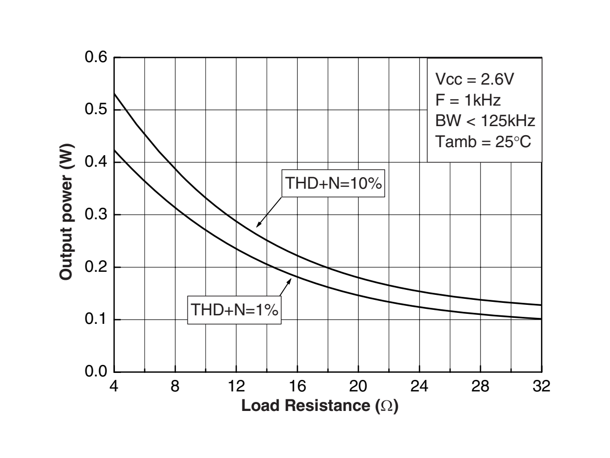


Figure 29. Output power vs. power supply voltage

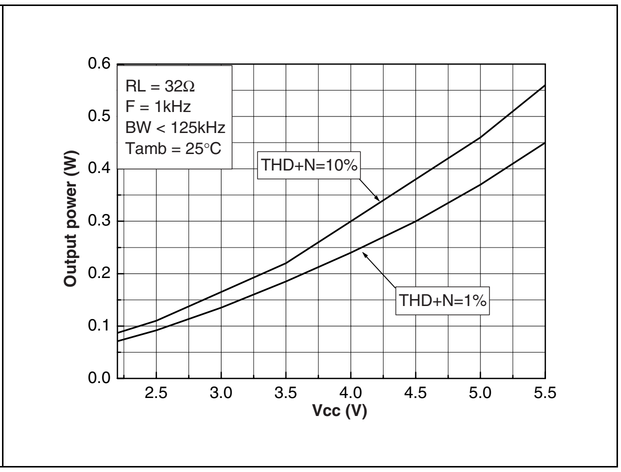


Figure 30. Output power vs. load resistor

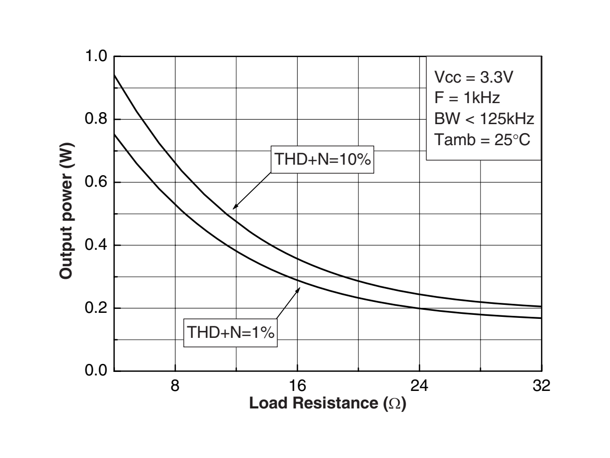


Figure 31. Power dissipation vs. P_{out}

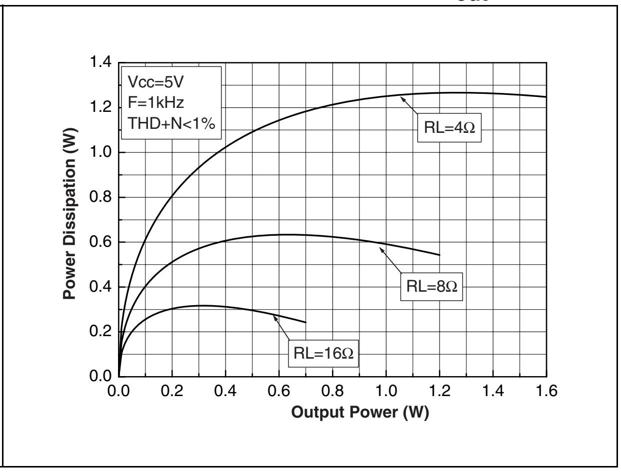


Figure 32. Power dissipation vs. P_{out}

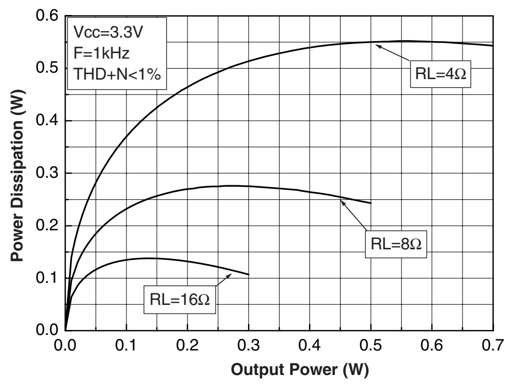


Figure 33. Power derating curves

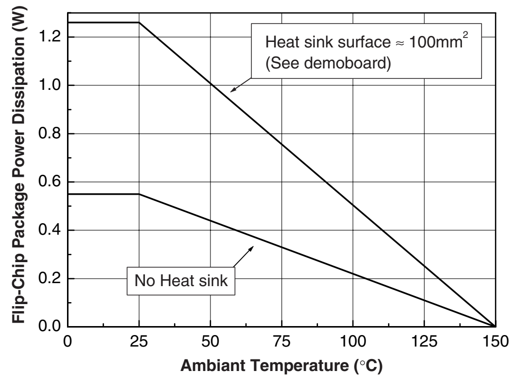


Figure 34. Clipping voltage vs. power supply voltage and load resistor

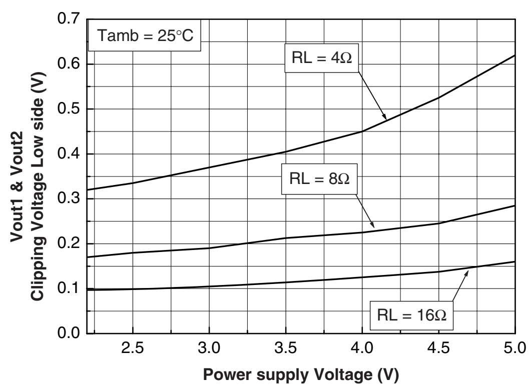


Figure 35. Power dissipation vs. P_{out}

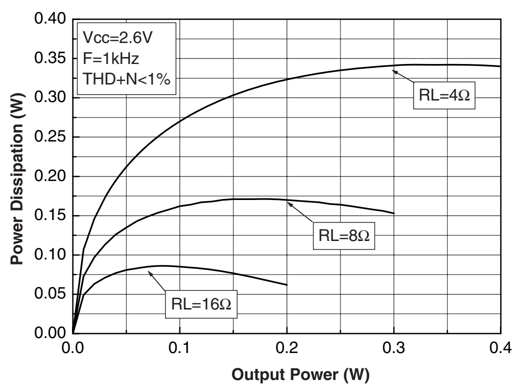


Figure 36. Clipping voltage vs. power supply voltage and load resistor

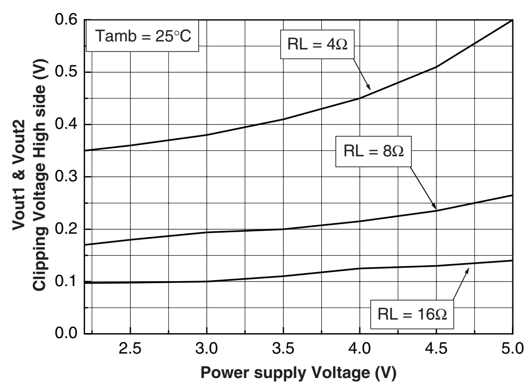


Figure 37. Current consumption vs. power supply voltage

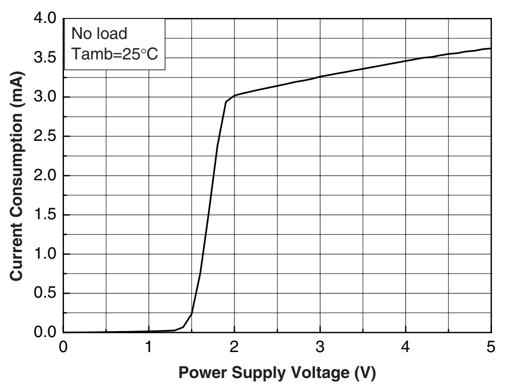


Figure 38. Current consumption vs. standby voltage @ V_{CC} = 5V

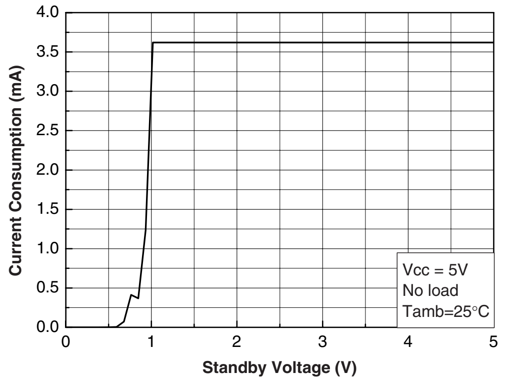


Figure 39. Current consumption vs. standby voltage @ V_{CC} = 2.6V

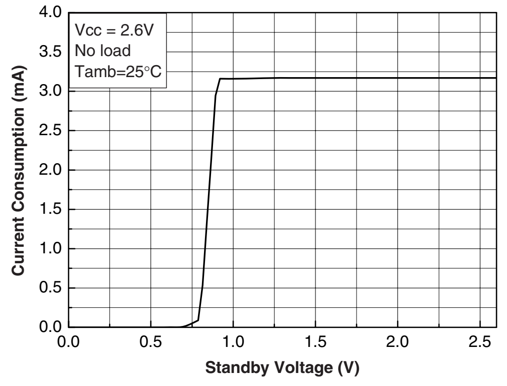


Figure 40. THD + N vs. output power

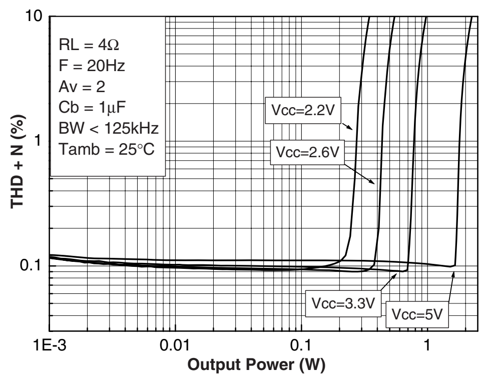


Figure 41. Current consumption vs. standby voltage @ V_{CC} = 3.3V

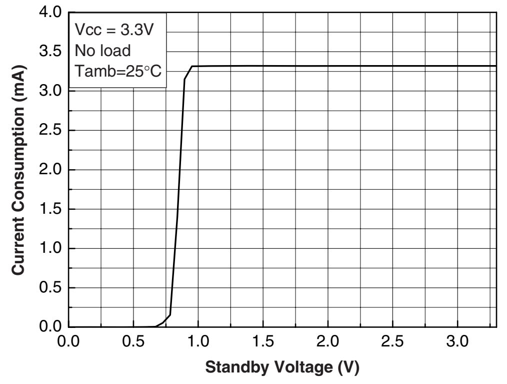


Figure 42. Current consumption vs. standby voltage @ V_{CC} = 2.2V

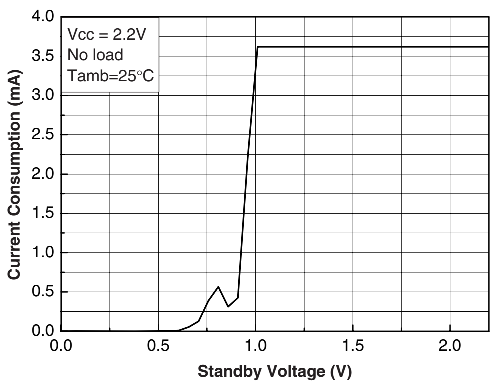


Figure 43. THD + N vs. output power

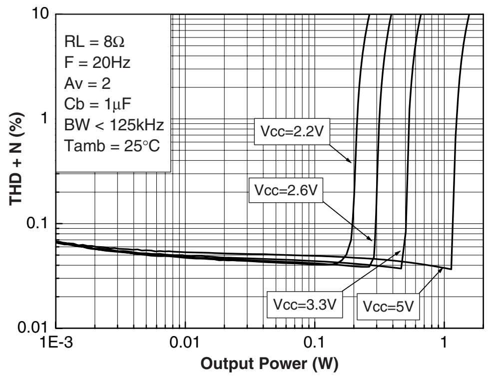


Figure 44. THD + N vs. output power

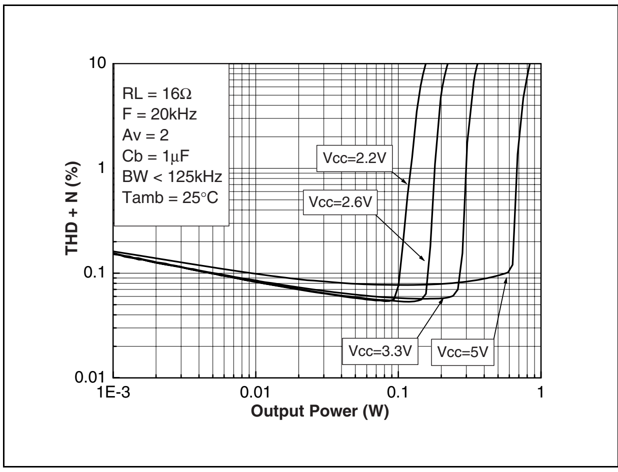


Figure 45. THD + N vs. output power

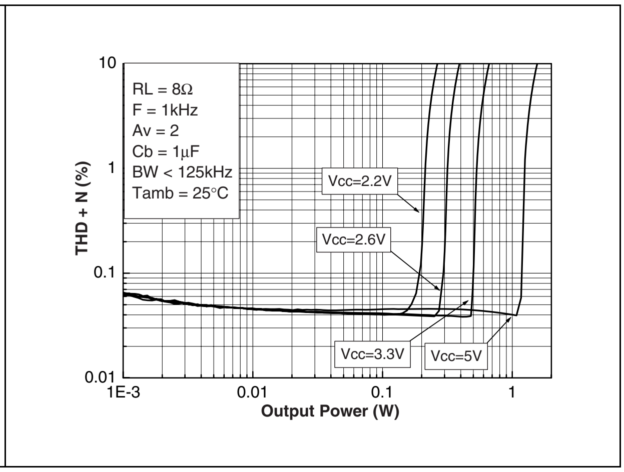


Figure 46. THD + N vs. output power

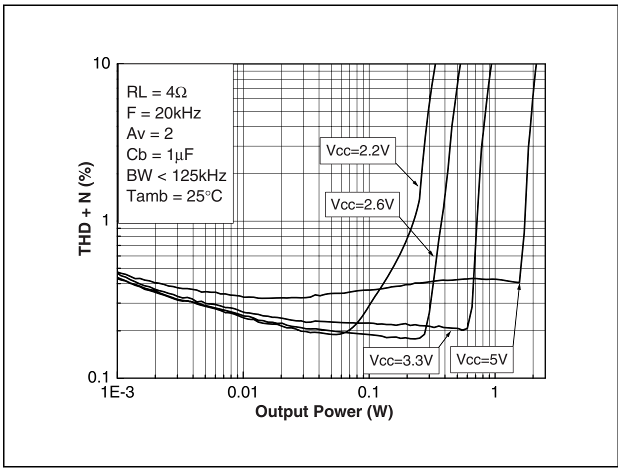


Figure 47. THD + N vs. output power

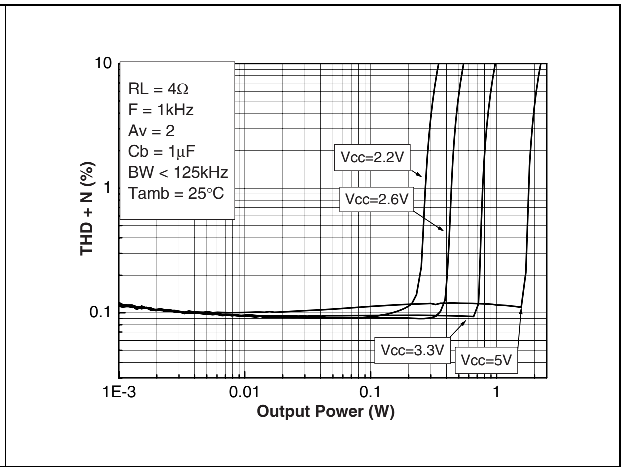


Figure 48. THD + N vs. output power

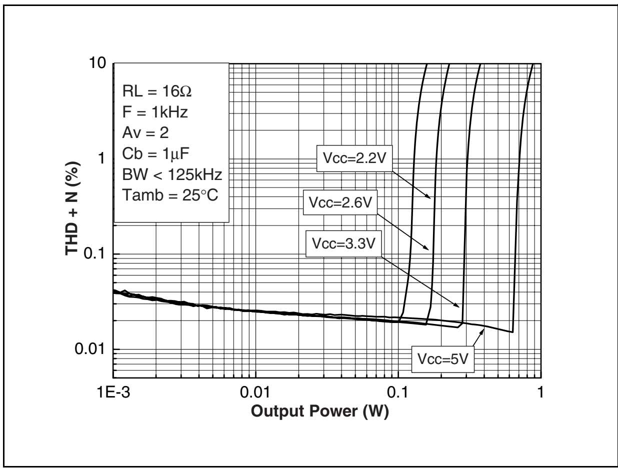


Figure 49. THD + N vs. output power

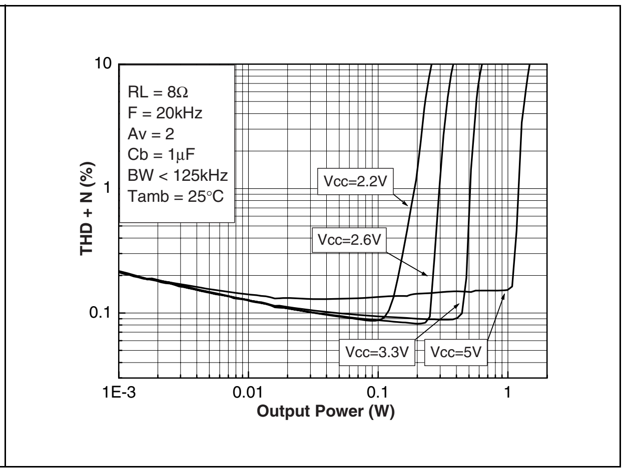


Figure 50. THD + N vs. output power

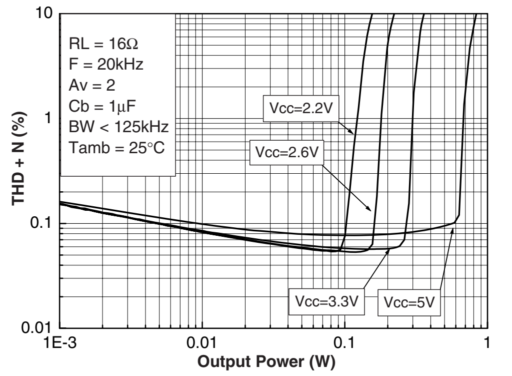


Figure 51. THD + N vs. frequency

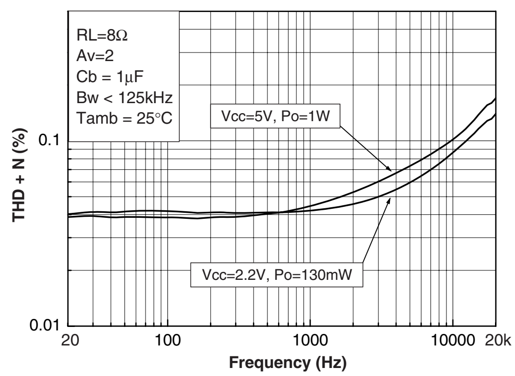


Figure 52. SNR vs. power supply with unweighted filter (20Hz to 20kHz)

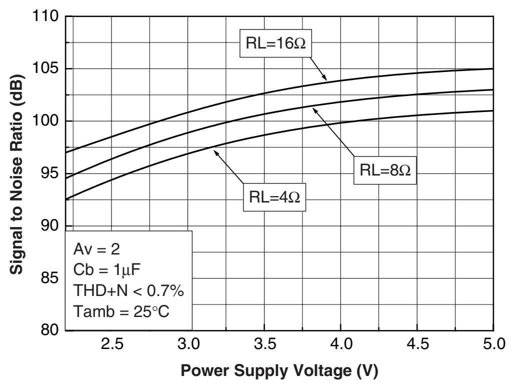


Figure 53. THD + N vs. frequency

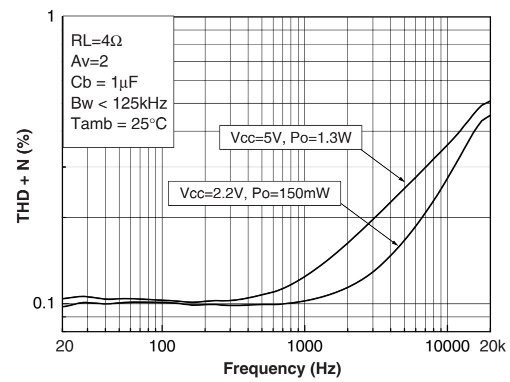


Figure 54. THD + N vs. frequency

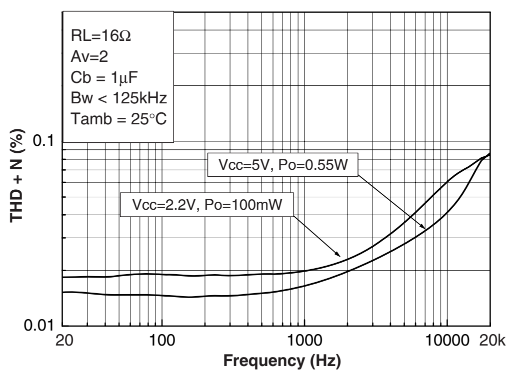


Figure 55. SNR vs. power supply with unweighted filter (20Hz to 20kHz)

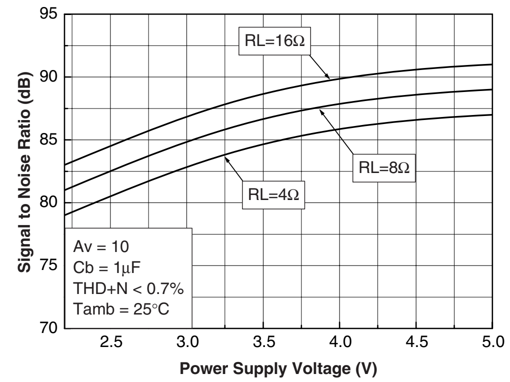


Figure 56. Signal to noise ratio vs. power supply with a weighted filter

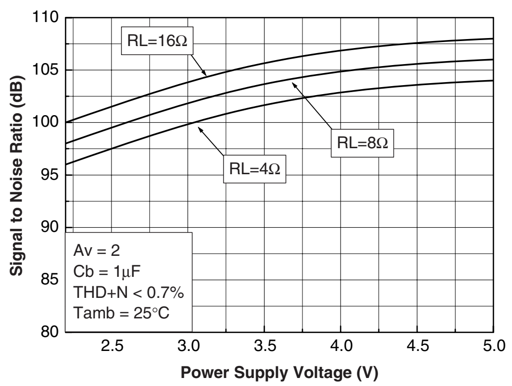


Figure 57. Output noise voltage device ON

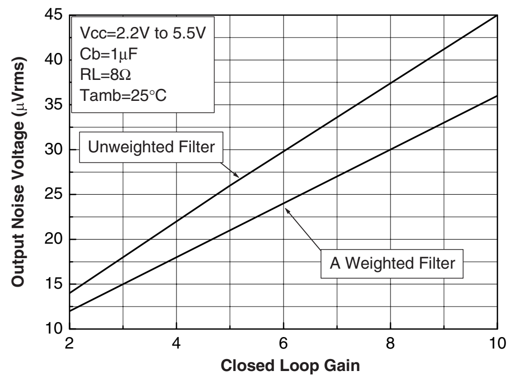


Figure 58. Signal to noise ratio vs. power supply with a weighted filter

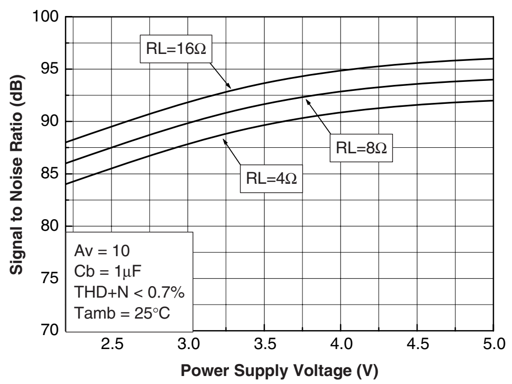
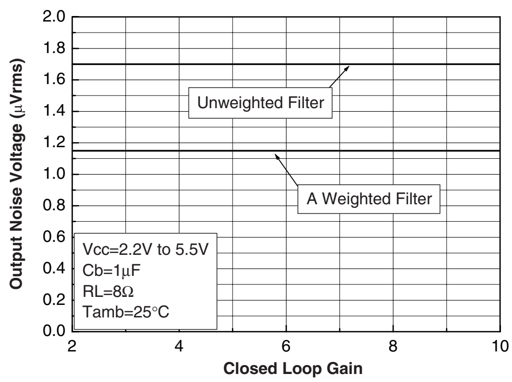


Figure 59. Output noise voltage device in Standby



4 Application information

4.1 BTL configuration principle

The TS4990 is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single-ended output 1 = $V_{out1} = V_{out}$ (V)
Single-ended output 2 = $V_{out2} = -V_{out}$ (V)

and $V_{out1} - V_{out2} = 2V_{out}$ (V)

The output power is:

$$P_{out} = \frac{(2V_{out_{RMS}})^2}{R_L}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single-ended configuration.

4.2 Gain in a typical application

The typical application schematics are shown in *Figure 1 on page 4*.

In the flat region (no C_{in} effect), the output voltage of the first stage is (in Volts):

$$V_{out1} = (-V_{in})\frac{R_{feed}}{R_{in}}$$

For the second stage: $V_{out2} = -V_{out1}$ (V)

The differential output voltage is (in Volts):

$$V_{out2} - V_{out1} = 2V_{in}\frac{R_{feed}}{R_{in}}$$

The differential gain named gain (G_v) for more convenience is:

$$G_v = \frac{V_{out2} - V_{out1}}{V_{in}} = 2\frac{R_{feed}}{R_{in}}$$

V_{out2} is in phase with V_{in} and V_{out1} is phased 180° with V_{in}. This means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1}.

4.3 Low and high frequency response

In the low frequency region, C_{in} starts to have an effect. C_{in} forms with R_{in} a high-pass filter with a -3 dB cut-off frequency. F_{CL} is in Hz.

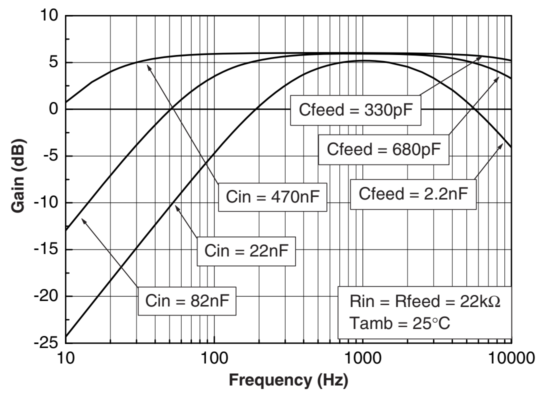
$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}}$$

In the high frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel with R_{feed}. It forms a low-pass filter with a -3 dB cut-off frequency. F_{CH} is in Hz.

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}}$$

The graph in *Figure 60* shows an example of C_{in} and C_{feed} influence.

Figure 60. Frequency response gain vs. C_{in} and C_{feed}



4.4 Power dissipation and efficiency

Hypotheses:

- Load voltage and current are sinusoidal (V_{out} and I_{out}).
- Supply voltage is a pure DC source (V_{CC}).

The load can be expressed as:

$$V_{out} = V_{PEAK}\sin\omega t \qquad (V)$$

and

$$I_{out} = \frac{V_{out}}{R_L} \qquad (A)$$

and

$$P_{out} = \frac{{V_{PEAK}}^2}{2R_L} \qquad (W)$$

Therefore, the average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = 2\frac{V_{PEAK}}{\pi R_L} \qquad (A)$$

The power delivered by the supply voltage is:

$$P_{supply} = V_{CC} \cdot I_{CC_{AVG}} \qquad (W)$$

Therefore, the **power dissipated by each amplifier** is:

$P_{diss} = P_{supply} - P_{out}$ (W)

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\delta P_{diss}}{\delta P_{out}} = 0$$

and its value is:

$$P_{diss_{max}} = \frac{2V_{CC}^2}{\pi^2 R_L} \quad \text{(W)}$$

Note: This maximum value is only dependent on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{PEAK} = V_{CC}$, so:

$$\frac{\pi}{4} = 78.5\%$$

4.5 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4990: a power supply bypass capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has particular influence on the THD+N in the high frequency region (above 7 kHz) and an indirect influence on power supply disturbances. With a value for C_s of 1 µF, you can expect THD+N levels similar to those shown in the datasheet.

In the high frequency region, if C_s is lower than 1 µF, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_s is higher than 1 µF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_b is lower than 1 µF, THD+N increases at lower frequencies and PSRR worsens.

If C_b is higher than 1 µF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

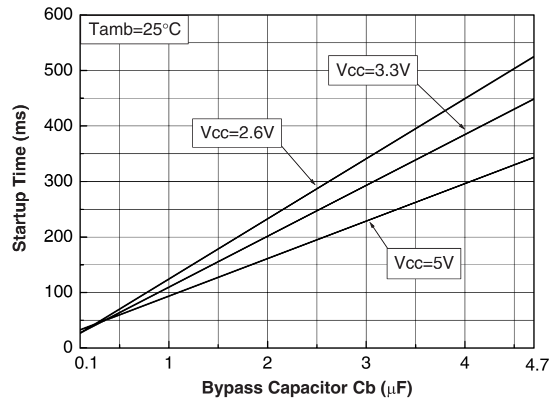
Note that C_{in} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{in}, the higher the PSRR.

4.6 Wake-up time (t_{WU})

When the standby is released to put the device ON, the bypass capacitor C_b is not charged immediately. Because C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called wake-up time or t_{WU} and specified in the electrical characteristics tables with C_b = 1 µF.

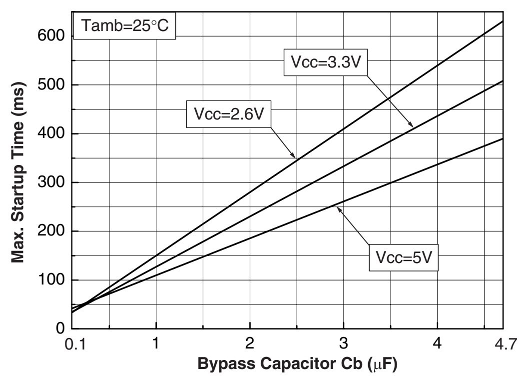
If C_b has a value other than 1 µF, refer to the graph in *Figure 61* to establish the wake-up time.

Figure 61. Typical wake-up time vs. C_b



Due to process tolerances, the maximum value of wake-up time is shown in *Figure 62*.

Figure 62. Maximum wake-up time vs. C_b



Note: The bypass capacitor C_b also has a typical tolerance of +/-20%. To calculate the wake-up time with this tolerance, refer to the graph above (considering for example for C_b=1 µF in the range of 0.8 µF≤ C_b≤ 1.2 µF).

4.7 Standby time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in standby mode is a few microseconds. In standby mode, the bypass pin and V_{in} pin are short-circuited to ground by internal switches. This allows a quick discharge of C_b and C_{in} capacitors.

4.8 Pop performance

Pop performance is intimately linked with the size of the input capacitor C_{in} and the bias voltage bypass capacitor C_b.

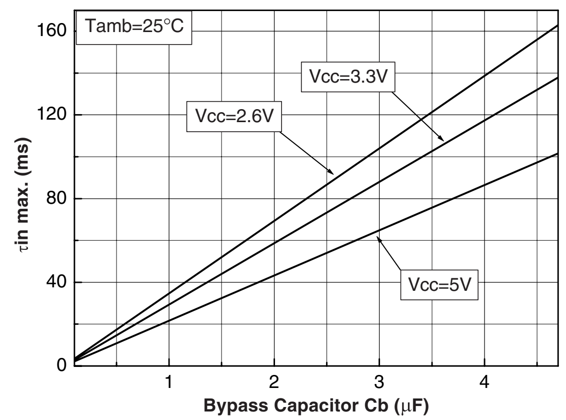
The size of C_{in} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_b is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_b determines the speed with which the amplifier turns ON. In order to reach near zero pop and click, the equivalent input constant time,

$$\tau_{in} = (R_{in} + 2k\Omega) \times C_{in} \text{ (s) with } R_{in} \geq 5k\Omega$$

must not reach the τ_{in} maximum value as indicated in *Figure 63* below.

Figure 63. τ_{in} max. versus bypass capacitor



By following the previous rules, the TS4990 can reach near zero pop and click even with high gains such as 20 dB.

Example:

With R_{in} = 22 kΩ and a 20 Hz, -3 dB low cut-off frequency, C_{in} = 361 nF. So, C_{in} = 390 nF with standard value which gives a lower cut-off frequency equal to 18.5 Hz. In this case, $(R_{in} + 2k\Omega) \times C_{in}$ = 9.36ms. By referring to the previous graph, if C_b = 1 µF and V_{CC} = 5 V, we read 20 ms max. This value is twice as high as our current value, thus we can state that pop and click will be reduced to its lowest value.

Minimizing both C_{in} and the gain benefits both the pop phenomenon, and the cost and size of the application.

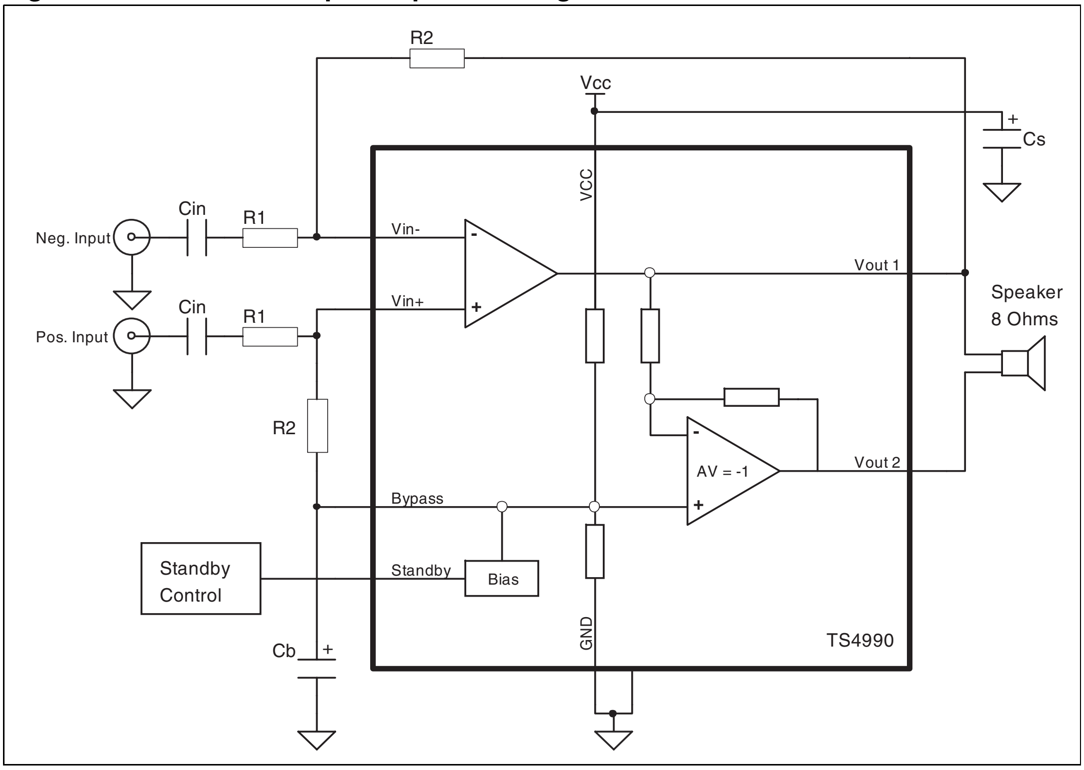
4.9 Application example: differential input, BTL power amplifier

The schematics in *Figure 64* show how to configure the TS4990 to work in differential input mode. The gain of the amplifier is:

$$G_{VDIFF} = 2\frac{R_2}{R_1}$$

In order to reach the best performance of the differential function, R_1 and R_2 should be matched at 1% max.

Figure 64. Differential input amplifier configuration



The input capacitor C_{in} can be calculated by the following formula using the -3 dB lower frequency required. (F_L is the lower frequency required).

$$C_{in} \approx \frac{1}{2\pi R_1 F_L} \quad (F)$$

Note: *This formula is true only if:*

$$F_{CB} = \frac{1}{2\pi(R_1 + R_2)C_B} \quad (Hz)$$

is 5 times lower than F_L.

Example bill of materials

The bill of materials in *Table 7* is for the example of a differential amplifier with a gain of 2 and a -3 dB lower cut-off frequency of about 80 Hz.

Table 7. Bill of materials for differential input amplifier application

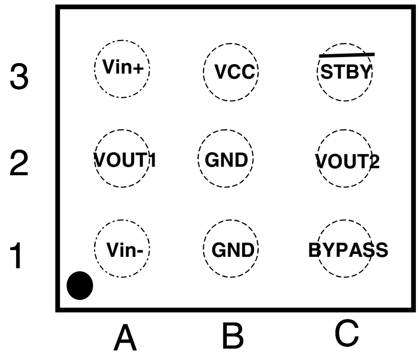
Pin name	Functional description
R_1	20k / 1%
R_2	20k / 1%
C_{in}	100 nF
C_b=C_s	1 µF
U1	TS4990

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

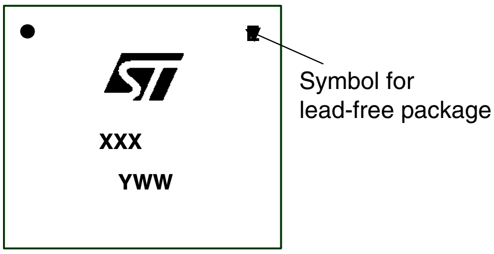
5.1 Flip-chip package information

Figure 65. Flip-chip pinout (top view)



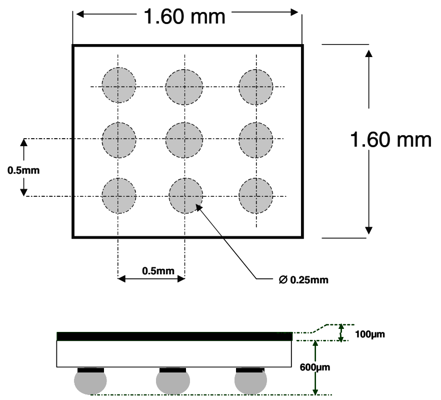
- Balls are underneath

Figure 66. Marking (top view)



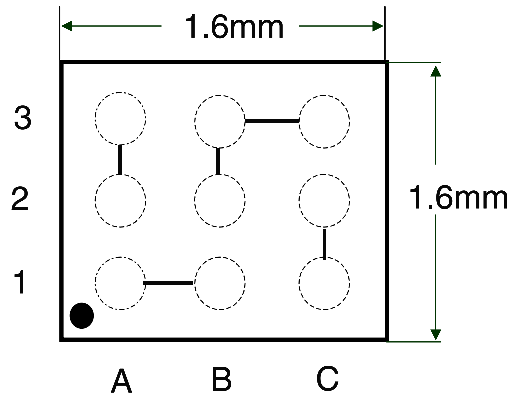
- ST logo
- Product and assembly code: XXX
  A90 from Tours
  90S from Shenzhen
- Three-digit datecode: YWW
- E symbol for lead-free only
- The dot indicates pin A1

Figure 67. Package mechanical data for 9-bump flip-chip package



- Die size: **1.60 x 1.60 mm ±30µm**
- Die height (including bumps): **600µm**
- Bump diameter: **315µm ±50µm**
- Bump diameter before reflow: **300µm ±10µm**
- Bump height: **250µm ±40µm**
- Die height: **350µm ±20µm**
- Pitch: **500µm ±50µm**
- Coplanarity: **50µm max**
- * Back coating height: **100µm ±10µm**
  * Optional

Figure 68. Daisy chain mechanical data



The daisy chain sample features two-by-two pin connections. The schematics in *Figure 68* illustrate the way pins connect to each other. This sample is used to test continuity on your board. Your PCB needs to be designed the opposite way, so that pins that are unconnected in the daisy chain sample, are connected on your PCB. If you do this, by simply connecting an Ohmmeter between pin A1 and pin A3, the soldering process continuity can be tested.

Figure 69. TS4990 footprint recommendations

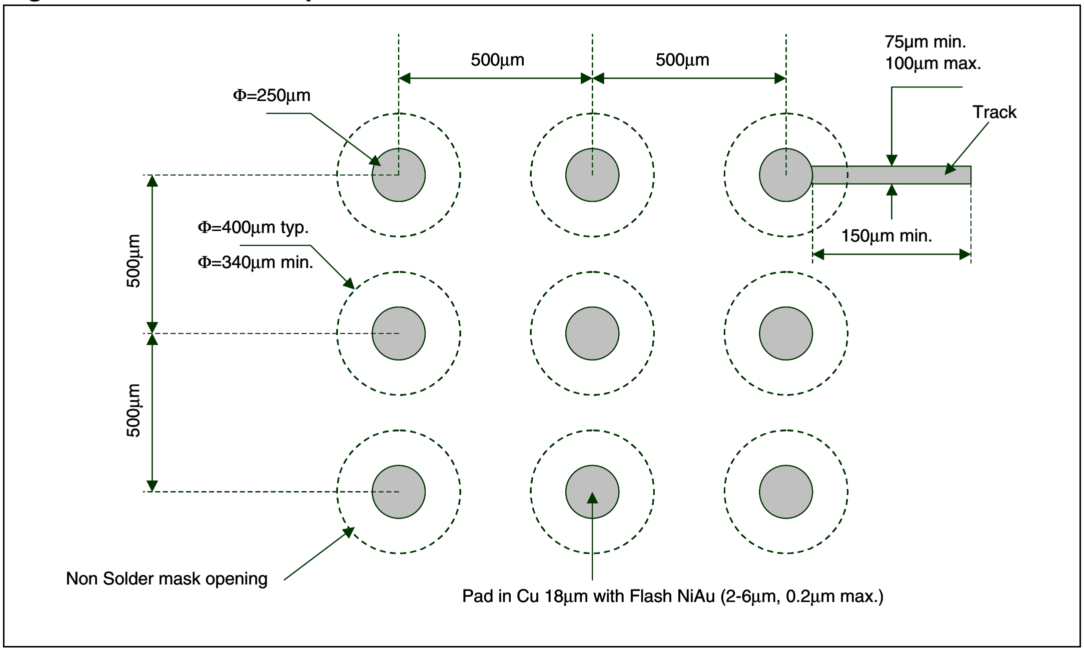
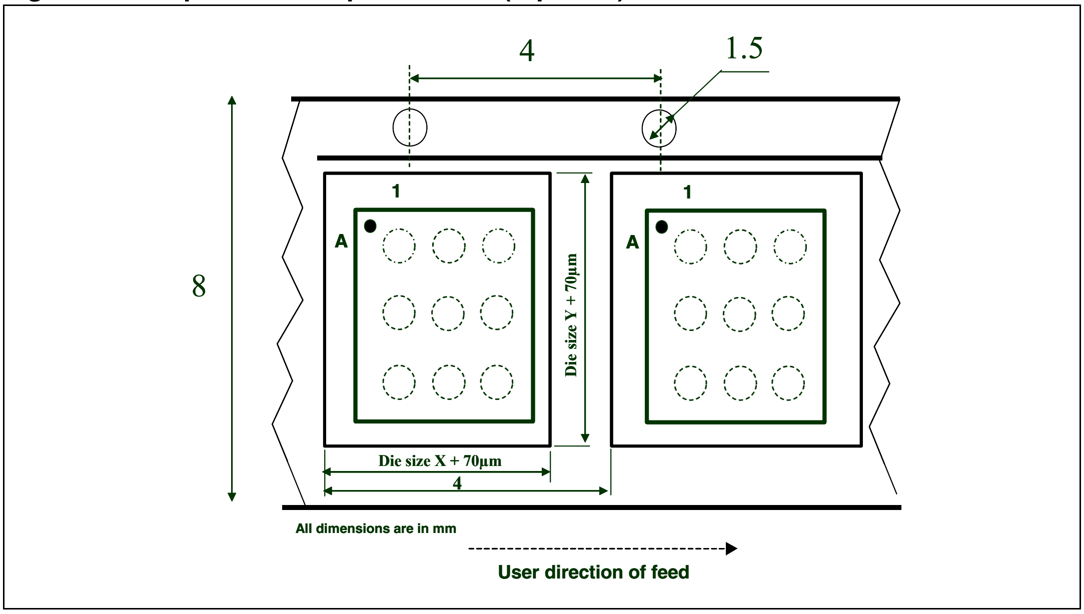


Figure 70. Tape and reel specification (top view)



Device orientation

The devices are oriented in the carrier pocket with pin number A1 adjacent to the sprocket holes.

5.2 MiniSO-8 package information

Figure 71. MiniSO-8 package mechanical drawing

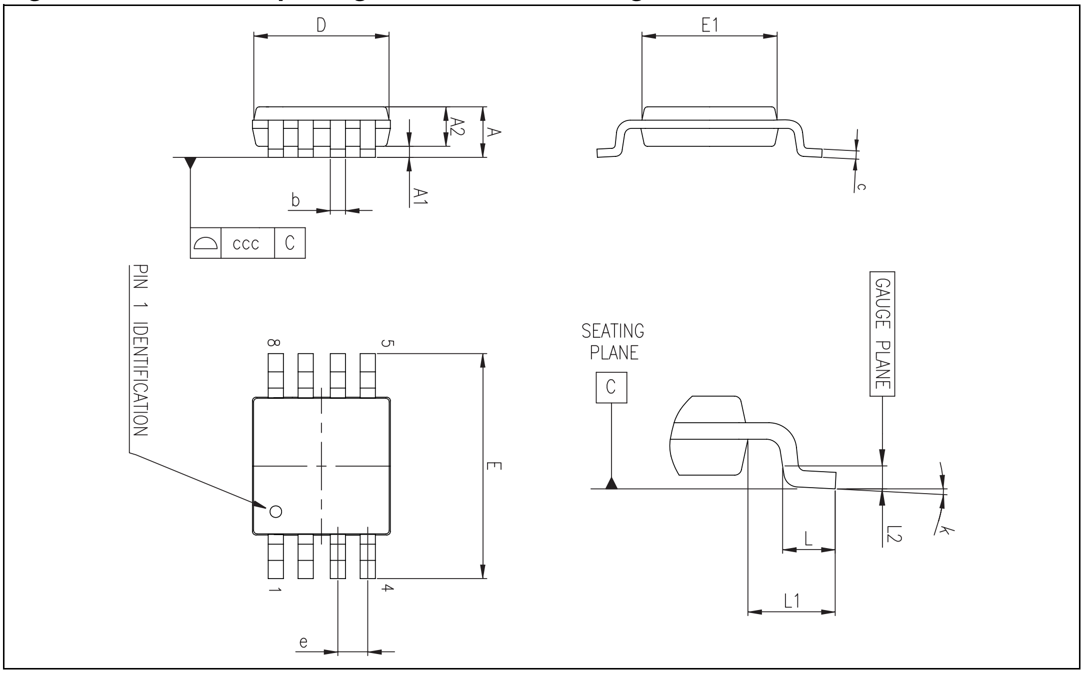


Table 8. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

5.3 DFN8 package information

Note: DFN8 exposed pad (E2 x D2) is connected to pin number 7. For enhanced thermal performance, the exposed pad must be soldered to a copper area on the PCB, acting as a heatsink. This copper area can be electrically connected to pin7 or left floating.

Figure 72. DFN8 3x3x0.90mm package mechanical drawing (pitch 0.5mm)

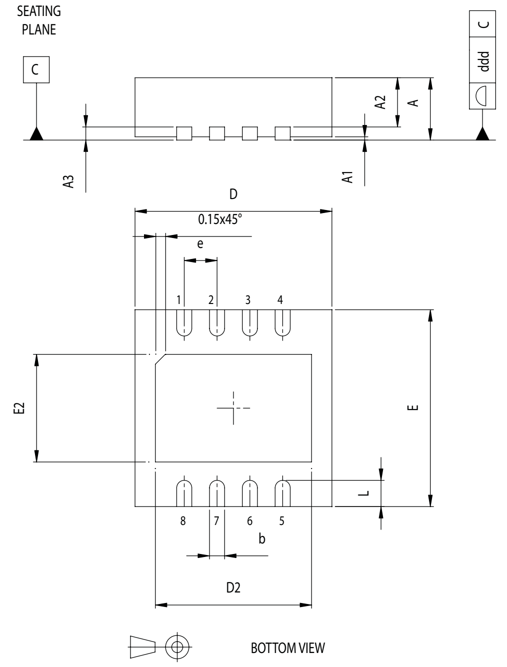


Table 9. DFN8 3x3x0.90mm package mechanical data (pitch 0.5mm)

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2	0.55	0.65	0.80	217	25.6	31.5
A3		0.20			7.9	
b	0.18	0.25	0.30	7.1	9.8	11.8
D	2.85	3.00	3.15	112.2	118.1	124
D2	2.20		2.70	86.6		106.3
E	2.85	3.00	3.15	112.2	118.1	124
E2	1.40		1.75	55.1		68.9
e		0.50			19.7	
L	0.30	0.40	0.50	11.8	15.7	19.7
ddd			0.08			3.1

5.4 SO-8 package information

Figure 73. SO-8 package mechanical drawing

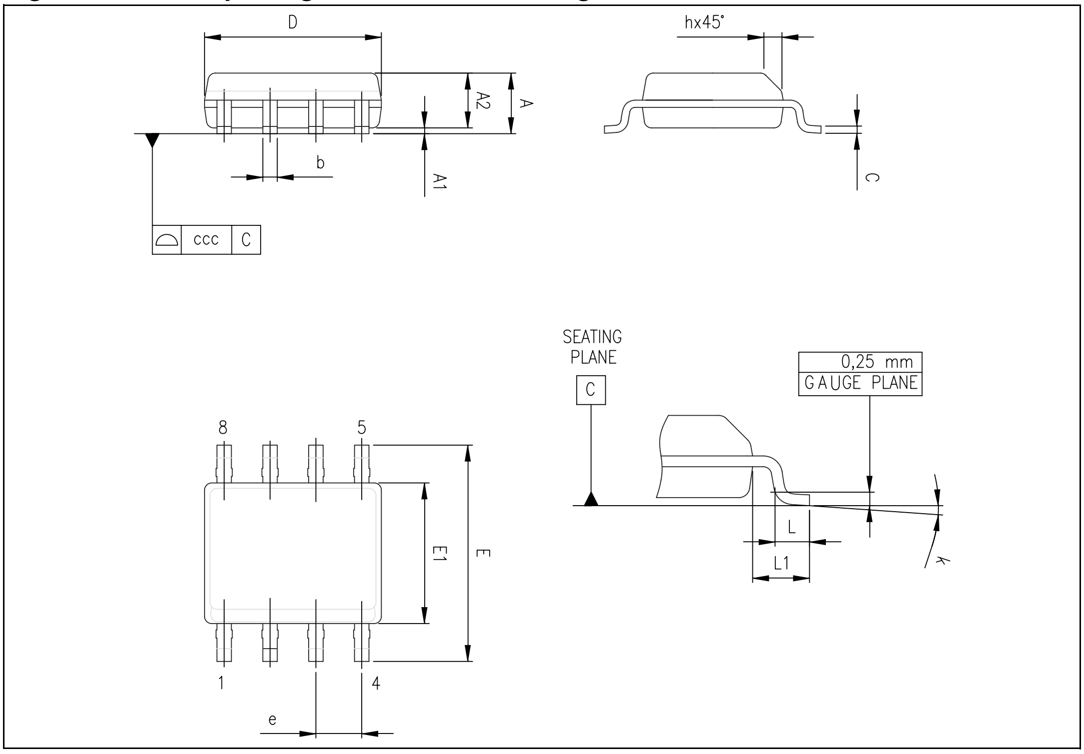


Table 10. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
H	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

6 Ordering information

Table 11. Order codes

Order code	Temperature range	Package	Packing	Marking
TS4990IJT TS4990EIJT[1]	-40°C, +85°C	Flip-chip, 9 bumps	Tape & reel	90
TSDC05IJT TSDC05EIJT[2]		Flip-chip, 9 bumps	Tape & reel	DC3
TS4990IST		MiniSO-8	Tape & reel	K990
TS4990IQT		DFN8	Tape & reel	K990
TS4990EKIJT		FC + back coating	Tape & reel	90
TS4990ID TS4990IDT		SO-8	Tube or Tape & reel	TS4990I

1. Lead-free Flip-chip part number
2. Lead-free daisy chain part number

7 Revision history

Table 12. Document revision history

Date	Revision	Changes
1-Jul-2002	1	First release.
4-Sep-2003	2	Update mechanical data.
1-Oct-2004	3	Order code for back coating on flip-chip.
2-Apr-2005	4	Typography error on page 1: Mini-SO-8 pin connection.
May-2005	5	New marking for assembly code plant.
1-Jul-2005	6	Error on *Table 4 on page 5*. Parameters in wrong column.
28-Sep-2005	7	Updated mechanical coplanarity data to 50µm (instead of 60µm) (see *Figure 67 on page 25*).
14-Mar-2006	8	SO-8 package inserted in the datasheet.
21-Jul-2006	9	Update of *Figure 66 on page 25*. Disclaimer update.
11-May-2007	10	Corrected value of PSRR in *Table 5 on page 6* from 1 to 61 (typical value). Moved *Table 3: Component descriptions* to *Section 2: Typical application schematics on page 4*. Merged daisy chain flip-chip order code table into *Table 11: Order codes on page 31*.
17-Jan-2008	11	Corrected pitch error in DFN8 package information. Actual pitch is 0.5mm. Updated DFN8 package dimensions to correspond to JEDEC databook definition (in previous versions of datasheet, package dimensions were as in manufacturer's drawing). Corrected error in MiniSO-8 package information (L and L1 values were inverted). Reformatted package information.
21-May-2008	12	Corrected value of output resistance vs. ground in standby mode: removed from *Table 2*, and added in *Table 4*, *Table 5*, and *Table 6*.
30-Aug-2011	13	Updated DFN8 package (*Figure 72*) Updated ECOPACK® text in *Section 5: Package information*